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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,020	06/30/2003	Ichiro Mizushima	04329.3083	1912
7590	08/27/2004		EXAMINER	
Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P. 1300 I Street, N.W. Washington, DC 20005-3315				KESHAVAN, BELUR V
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,020	MIZUSHIMA, ICHIRO	
	Examiner	Art Unit	
	Belur V Keshavan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 June 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 June 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/5/04, 10/20/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (Pub. NO: JP401152274A, titled “Method For Removing Pollutant After Chlorine Fluoride Cleaning In Film Forming Operation System.”).

Regarding claims 1 and 2 Watanabe et al. disclose in the Abstract a method of purging a CVD-deposited film deposited in a chamber constituting a semiconductor manufacturing apparatus which has performed a process of forming a CVD film using a CVD method over a semiconductor wafer, by using an etching gas which contains at least a halogen gas; and a step of purging a cleaning gas remaining in the chamber by causing a gas containing a mixture hydrogen and nitrogen to flow into the chamber after the step of etching the CVD deposited film by using the cleaning gas.

Regarding claim 4, Watanabe et al. disclose in the Abstract wherein the cleaning gas in the step of etching is a ClF₃ gas, which contains at least a halogen gas.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. Watanabe et al. anticipates claims 1 and 2 as above but lack the contents of hydrogen and nitrogen gases in the mixture of hydrogen and nitrogen gasses purging the semiconductor manufacturing apparatus. It would have been obvious to one having ordinary skill in the art at the time the invention was made to discover the optimum contents of hydrogen and nitrogen gases in the purging gas mixture as it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. Watanabe et al. anticipates claim 1 and 2 as above. Watanabe et al. disclose a process of purging a CVD apparatus, a semiconductor manufacturing apparatus, after a dry cleaning step as given above but lack a step of mounting a semiconductor wafer in the apparatus after disclosed purging

and a step of forming a CVD film over the semiconductor wafer mounted in the chamber. As the apparatus is a CVD apparatus and dry cleaning step is done after forming CVD film in the apparatus it is obvious to a person of ordinary skill in the art at the time the invention was made to use the purge cleaned CVD apparatus to form a CVD film over the semiconductor wafer mounted in the chamber of the CVD apparatus.

Claim Rejections - 35 USC § 102

Claims 5, 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiba (PUB. NO. JP405259133A, titled “Dry Etching Apparatus And Cleaning Method Therefor”).

Regarding claims 5 and 6 Chiba discloses, in the Abstract, in paragraph [0010] and in paragraph [0019], a method of purging a CVD-deposited film deposited in a chamber constituting a semiconductor manufacturing apparatus which has performed a process of forming a CVD film using a CVD method over a semiconductor wafer, by using an etching gas which contains at least a halogen gas; and a step of purging a cleaning gas remaining in the chamber by causing a gas containing a mixture of water vapor and nitrogen to flow into the chamber after the step of etching the CVD deposited film by using the cleaning gas.

Regarding claim 8, Chiba discloses in paragraph [0010], wherein the cleaning gas in the step of etching is a ClF₃ gas.

Claim Rejections - 35 USC § 103

Claim 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba.

Regarding claim 7, Chiba anticipates claims 5 and 6 as above but lack the contents of water vapor and nitrogen gases in the mixture water vapor and nitrogen gasses purging the semiconductor manufacturing apparatus. It would have been obvious to one having ordinary skill

in the art at the time the invention was made to discover the optimum contents of water vapor and nitrogen gases in the purging gas mixture as it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 18, Chiba anticipates claims 5 and 6 as above. Chiba discloses a process of purging a CVD apparatus, a semiconductor manufacturing apparatus, after a dry cleaning step as given above but lack a step of mounting a semiconductor wafer in the apparatus after disclosed purging and a step of forming a CVD film over the semiconductor wafer mounted in the chamber. As the apparatus is a CVD apparatus and dry cleaning step is done after forming CVD film in the apparatus it is obvious to a person of ordinary skill in the art at the time the invention was made to use the purge cleaned CVD apparatus to form a CVD film over the semiconductor wafer mounted in the chamber of the CVD apparatus.

Claim Rejections - 35 USC § 102

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Nagashima et al. (U.S. Patent No. 5,129,958).

Regarding claim 9, Nagashima et al. discloses, in column 2 and lines 21-53 a method of purging a semiconductor manufacturing apparatus, comprising: a step of etching a CVD-deposited film deposited in a chamber constituting a semiconductor manufacturing apparatus which has performed a process of forming a CVD film using a CVD process over a semiconductor wafer, by using an etching gas which contains at least a halogen gas; and a step of purging a cleaning gas remaining in the chamber by causing a gas containing a substance, which

becomes alkaline upon being dissolved in water to flow into the chamber after the step of etching the CVD deposited film by using the cleaning gas.

Claim Rejections - 35 USC § 103

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashima et al. and in view of Watanabe.

Regarding claim 10, Nagashima et al. anticipate claim 9 as above but lack mixing nitrogen with the gas containing the substance that becomes alkali upon being dissolved in water in the step of purging. However, Watanabe et al. disclose using nitrogen gas as a dilutant gas for purging gas. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to mix the gas containing the substance that becomes alkali upon being dissolved in water with nitrogen as purging gas as the dilutant nitrogen would facilitate the flushing of residues in the CVD chamber.

Regarding claim 11, Nagashima et al. anticipate claim 9 as above but lack ClF₃ gas as an etching gas. However, Watanabe discloses the use of a ClF₃ gas as an etchant. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Nagashima et al. with that of Watanabe and use a ClF₃ gas for etch cleaning as it would facilitate the removal of the CVD deposition residues in the CVD chamber.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashima et al.

Regarding claim 19, Nagashima et al. anticipates claims 9 as above. Nagashima et al. discloses a process of purging a CVD apparatus, a semiconductor manufacturing apparatus, after a dry cleaning step as given above but lack a step of mounting a semiconductor wafer in the apparatus after disclosed purging and a step of forming a CVD film over the semiconductor

wafer mounted in the chamber. As the apparatus is a CVD apparatus and dry cleaning step is done after forming CVD film in the apparatus it is obvious to a person of ordinary skill in the art at the time the invention was made to use the purge cleaned CVD apparatus to form a CVD film over the semiconductor wafer mounted in the chamber of the CVD apparatus.

Claim Rejections - 35 USC § 102

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Nagashima et al. (U.S. Patent No. 5,129,958).

Regarding claim 12, Nagashima et al. discloses, in column 2, lines 21-53, a method of purging a semiconductor manufacturing apparatus comprising; a step of etching a CVD-deposited film deposited in a chamber constituting a semiconductor manufacturing apparatus which has performed a process of forming a CVD film using a CVD process over a semiconductor wafer by using an etching gas containing at least a halogen gas; and a step of purging a cleaning gas remaining in the chamber by causing ammonia to flow into the chamber after the step of etching the CVD-deposited film by using the cleaning gas.

Claim Rejections - 35 USC § 103

Claims 13 and 15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashima et al. and in view of Watanabe.

Regarding claim 13, Nagashima et al. anticipates claim 12 as above but lack mixing nitrogen with ammonia as the purging gas. However, Watanabe et al. disclose using nitrogen gas as a dilutant gas for purging gas. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to mix ammonia with nitrogen as purging gas

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as the mixture of nitrogen and ammonia would facilitate the flushing of residues in the CVD chamber.

Regarding claim 15, Nagashima et al. anticipate claim 12 as above but lack ClF₃ gas as an etching gas. However, Watanabe discloses the use of a ClF₃ gas as an etchant. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Nagashima et al. with that of Watanabe and use a ClF₃ gas for etch cleaning as it would facilitate the removal of the CVD deposition residues in the CVD chamber.

Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashima

Regarding claim 16, Nagashima et al anticipates claim 12 above but lack the temperature in the chamber when ammonia is caused to flow into the chamber is about 800°C. It would have been obvious to one having ordinary skill in the art at the time the invention was made to establish optimum temperature in the chamber when ammonia is caused to flow into the chamber by experiment, as it has been held that discovering an optimum value or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagashima.

Regarding claim 20, Nagashima et al. anticipates claim 12 as above and discloses a method of cleaning a semiconductor wafer processing apparatus after it has been used in processing a semiconductor wafer to deposit a CVD film over the semiconductor wafer. Nagashima et al. lack a step of mounting a semiconductor wafer in a chamber of the purge cleaned semiconductor manufacturing apparatus (according to claim 12) and a step of forming a CVD film over the semiconductor wafer mounted in the chamber. However it is obvious to a

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person of ordinary skill in the art at the time the invention was made to use a cleaned apparatus for processing a semiconductor wafer to manufacture reliable devices with high yield.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 571-272-1894. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BVK.
August 26, 2004.

Belur V. Keshavan.
Examiner. Art Unit 2825.


Olik Chaudhuri
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